IN THE CLAIMS:

Listing of claims:

1-3. (canceled)

4. (currently amended) A method for manufacturing a semiconductor device having a trench element isolation region including a trench and a trench insulating layer that fills the trench, the method comprising the steps of:

(A) forming a pad oxide layer on a substrate;

(B) forming a polishing stopper layer on the pad oxide layer, the polishing stopper layer having a predetermined pattern for a chemical-mechanical polishing, the pad oxide layer positioned between the substrate and the polishing stopper layer;

(C) removing a part of the pad oxide layer and the substrate using a mask layer including at least the polishing stopper layer as a mask to form a trench;

(D) forming a trench oxide film on a surface of the substrate that forms the trench;

(E) forming an insulating layer that fills the trench;

(F) polishing the insulating layer by a chemical-mechanical polishing;

(G) removing the polishing stopper layer;

(H) etching a part of the insulating layer to form a trench insulating layer and etching the pad oxide layer remaining on the substrate adjacent to the trench; and

(I) after the etching the remaining pad <u>oxide</u> layer, forming a sacrificial oxide layer on the substrate adjacent to the trench;

wherein the method further includes the step (a) of forming an etching stopper layer for the trench oxide film over at least a portion of the trench oxide film, wherein the etching stopper layer is a silicon nitride layer and wherein, in the step (H), the etching stopper layer is more resistant to the etching than the insulating layer;

<u>wherein the etching stopper layer is formed to have an upper surface that is positioned no higher than an upper surface of the sacrificial oxide layer; and</u>

<u>after the sacrificial oxide is formed, implanting an impurity into the substrate, and then removing the sacrificial oxide layer, wherein after the sacrificial oxide is removed, the insulating</u>

layer has an upper surface that is positioned higher than an upper surface of the etching stopper layer.

5. (original) A method for manufacturing a semiconductor device according claim 4, wherein the silicon nitride layer has a thickness of 10 – 50 nm.

6-29. (canceled)

30. (previously presented) A method as in claim 32, further comprising forming the trench so that an angle at an intersection between the lower surface of the trench and a side surface of the trench is greater than 90 degrees.

31. (canceled)

32. (previously presented) A method for manufacturing a semiconductor device, comprising:

forming a trench comprising a lower surface and side surfaces in a silicon substrate;

forming a trench oxide layer covering the lower surface and side surfaces;

forming rounded corner regions at an intersection of an upper surface of the substrate and the side surfaces of the trench;

forming an etch stop layer in direct contact with the trench oxide layer on the lower surface and side surfaces;

filling the trench with an insulating layer directly contacting the etch stop layer, wherein the insulating layer overfills the trench and a portion of the insulation layer extends over the upper surface of the substrate;

etching the insulating layer using an etchant that selectively etches the etch stop layer at a rate that is slower than that of the insulating layer, wherein the etching the insulating layer is carried out so that a first portion of the insulating layer that extends over the upper surface of the substrate is removed and a second portion of the insulating layer over the trench extends to a level above that of the upper surface of the substrate; and

after the etching the insulating layer, implanting an impurity into a first region of the silicon substrate, implanting an impurity into a second region of the silicon substrate, and after the implanting the impurity into the second region, etching the second portion of the insulating layer, wherein the etching is controlled so that the second portion of the insulating layer extends to a level above that of the upper surface of the substrate.

33. (previously presented) A method as in claim 32, further comprising forming an oxide layer on the upper surface of the substrate after the etching the insulating layer and prior to the implanting.

34. (currently amended) A method for manufacturing a semiconductor device, comprising:

forming a pad insulating layer on a silicon substrate;

forming a polishing stopper layer on the pad insulating layer;

forming a first resist layer having a specified pattern on the polishing stopper layer

etching the polishing stopper layer and the pad insulating layer using the first resist layer as a mask to yield a remaining polishing stopper layer and remaining pad insulation layer;

removing the first resist layer;

etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a trench in the silicon substrate;

oxidizing surfaces in the trench;

forming a silicon nitride layer on the oxidized surfaces in the trench;

forming an insulating layer on the silicon nitride layer and overfilling the trench;

planarizing the insulating layer that overfills the trench until the polishing stopper layer is reached;

removing the remaining polishing stopper layer;

etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer extends to a level higher than that of the silicon substrate; ~~and~~

performing at least one ion implantation while the insulation layer extends to a level higher than that of the silicon substrate; and

etching the insulation layer after the at least one ion implantation so that the insulation layer extends to a level higher than that of the silicon substrate.

35. (previously presented) A method as in claim 34, further comprising forming the trench so that an angle at an intersection between the lower surface of the trench and a side surface of the trench is greater than 90 degrees.

36. (currently amended) A method for manufacturing a semiconductor device, comprising:

forming a pad insulating layer on a silicon substrate;

forming a polishing stopper layer on the pad layer above an upper surface of the silicon substrate;

forming a first resist layer having a specified pattern on the polishing stopper layer;

etching the polishing stopper layer and the pad insulating layer using the first resist layer as a mask to yield a remaining polishing stopper layer and remaining pad insulation layer;

removing the first resist layer;

etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a trench in the silicon substrate;

oxidizing surfaces in the trench;

forming an etch stop layer on the oxidized surfaces in the trench and on side surfaces and an upper surface of the polishing stopper layer;

forming an insulating layer on the etch stop layer and overfilling the trench;

planarizing the insulating layer that overfills the trench;

after the planarizing, etching the polishing stopper layer and the etch stop layer so that the polishing stopper layer is removed and the etch stop layer that extends to a level above the upper surface of the silicon substrate is removed;

after the etching the polishing stopper layer, etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer remains at a level higher than that of the silicon substrate and the etch stop layer; ~~and~~

forming a sacrificial oxide layer on the silicon substrate;

performing at least one ion implantation into the silicon substrate while the insulation layer extends to a level higher than that of the silicon substrate and the etch stop layer; and

etching the sacrificial oxide layer and the insulation layer after the at least one ion implantation, wherein the etching is controlled so that the insulation layer extends to a level higher than that of the silicon substrate.

37. (previously presented) A method as in claim 36, wherein the etch stop layer comprises a silicon nitride layer.

38. (previously presented) A method as in claim 36, wherein the etch stop layer is a non-monocrystal silicon layer.

39. (previously presented) A method for manufacturing a semiconductor device according claim 36, wherein the non-monocrystal silicon layer is an amorphous silicon layer.

40. (previously presented) A method for manufacturing a semiconductor device according claim 36, wherein the non-monocrystal silicon layer is a polycrystal silicon layer.

41. (previously presented) A method for manufacturing a semiconductor device according claim 36, wherein the non-monocrystal silicon layer comprises a multi-layer structure including a polycrystal silicon layer and an amorphous silicon layer.

42. (previously presented) A method as in claim 36, wherein the etching the remaining pad insulation layer and the insulating layer includes isotropically etching the insulating layer.

43. (previously presented) A method as in claim 42, wherein the isotropically etching the insulating layer includes forming recessed side regions in the insulating layer adjacent to the silicon nitride layer.

44. (canceled)

45. (currently amended) A method as in claim [[44]]46, wherein the etch stop layer is a silicon nitride layer.

46. (currently amended) A method ~~as in claim 44,~~ for manufacturing a semiconductor device, comprising:

forming a pad insulating layer on a silicon substrate;

forming a polishing stopper layer on the pad layer above an upper surface of the silicon substrate;

etching the polishing stopper layer and the pad insulating layer using a mask to yield a remaining polishing stopper layer and remaining pad insulation layer;

etching the silicon substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a trench in the silicon substrate;

oxidizing surfaces in the trench;

forming an etch stop layer on the oxidized surfaces in the trench and on side surfaces and an upper surface of the polishing stopper layer;

forming an insulating layer on the etch stop layer and overfilling the trench;

planarizing the insulating layer that overfills the trench to a level that exposes the polishing stopper layer;

after the planarizing, etching the polishing stopper layer and the etch stop layer so that the polishing stopper layer is removed and the etch stop layer on the side surfaces of the polishing stopper layer is removed; and

after the etching the polishing stopper layer and the etch stop layer, etching the remaining pad insulation layer and the insulating layer so that a portion of the insulating layer remains at a level higher than that of the silicon substrate and the etch stop layer;

wherein the etch stop layer is formed from a non-monocrystal silicon layer selected from the group consisting of a polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.

47. (currently amended) A method for manufacturing a semiconductor device, comprising:

forming a pad insulating layer on a substrate;

forming a polishing stopper layer on the pad insulating layer, wherein the pad insulating layer is between the substrate and the polishing stopper layer;

etching the polishing stopper layer and the pad insulating layer using a mask to yield a remaining polishing stopper layer and remaining pad insulation layer;

etching the ~~silicon~~ substrate using the remaining polishing stopper layer and remaining pad insulation layer as a mask, to form a plurality of trenches in the substrate that are spaced apart from each other;

oxidizing surfaces in the trenches;

forming an etch stop layer on the oxidized surfaces in the trenches and on side surfaces and an upper surface of the remaining polishing stopper layer;

forming an insulating layer on the etch stop layer and overfilling the trenches;

planarizing the insulating layer that overfills the trenches to a level that exposes the remaining polishing stopper layer;

after the planarizing, etching the remaining polishing stopper layer and the etch stop layer so that the remaining polishing stopper layer is removed and the etch stop layer on the side surfaces of the remaining polishing stopper layer is removed;

after the etching the polishing stopper layer and the etch stop layer, etching the remaining pad insulation layer and a portion of the insulating layer so that the remaining pad insulation layer is removed and the substrate is exposed between the trenches; ~~and~~

after the etching the remaining pad insulation layer, forming an oxide layer on the exposed substrate between the trenches

performing at least one ion implantation into the substrate through the oxide layer; and

etching the oxide layer and the insulation layer after the at least one ion implantation, wherein the etching is controlled so that the insulation layer extends to a level higher than that of the substrate.

48. (currently amended) A method as in claim 47, wherein the etching the remaining pad insulation layer and a portion of the insulation layer is controlled so that a portion of the insulating layer remains at a level higher than that of ~~the substrate and~~ the etch stop layer.

49. (currently amended) A method as in claim 48, further comprising performing at least one ion implantation into the substrate while the insulation layer extends to a level higher than that of the ~~substrate and the~~ etch stop layer.

50. (new) A method as in claim 46, wherein the etch stop layer is formed from an amorphous silicon layer.

51. (new) A method as in claim 46, wherein the etch stop layer is formed from a polycrystal silicon layer.

52. (new) A method as in claim 46, wherein the etch stop layer is formed from a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.